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Accordingly, the power amplifier of the invention can provides a lower gate bias voltage (close to the operating range of a conventional class-AB or class B power amplifier) when the input power is low, and a higher gate bias voltage (close to the operating range of a conventional class-A power amplifier) when the input power is high. Therefore, the power amplifier of this invention has a high output power and linearity of operation as well as a high power-added efficiency regardless of whether the input power is low or high.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

FIG. 1 is a graph showing the relationships of output power, power gain and power-added efficiency versus input power of a conventional power amplifier.

FIG. 2 is a circuit diagram of a conventional semiconductor transistor power amplifier.

FIG. 3 is a circuit diagram of a power amplifier with an active bias circuit according to one embodiment of this invention.

FIG. 4 is a graph showing the relationship of the equivalent resistance versus the input power of a diode.

FIG. 5 is a graph showing the relationship of the gate bias voltage versus the input power for a power amplifier with active bias circuit of the invention and a conventional A-class power amplifier.

FIG. 6 is a graph showing the relationships of output power, power gain and power-added efficiency versus input power for a power amplifier with active bias circuit according to this invention and the similar relationships of a conventional class-A power amplifier.

FIG. 7 is a circuit diagram of a CMOS power amplifier with an active bias circuit according to one embodiment of this invention.

FIG. 8 is a graph showing the relationship of the output current versus the gate bias voltage of the two transistor circuits inside the active bias circuit according to one embodiment of this invention.

FIG. 9 is a graph showing the relationship of the drain-to-source current versus the input power of a power amplifier with an active bias circuit according to this invention and a conventional A-class power amplifier.

DESCRIPTION OF LABELS OF THE DRAWINGS

300, 700: power amplifier with active bias circuit

202, 302, 702, 712, 718: transistor

304, 704: active bias circuit

306: diode

308, 714, 716, 720: resistor

Pin: input power

Pout: output power

Vg, Vgb, Vgb1: gate bias voltage

L1, L2: curve